Thermal Management Modeling of High-power Chips and Calibration with Experimental Data

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The presented work follows previous activities in the area of thermal management of high-power semiconductor devices [1]. The goal of this activity is to carefully estimate the thermal conductivity of the die-attach layer, based on a realistic package model with a thermo-electric cooler. For a proper estimation, an inverse thermal problem is solved with a fully multi-physics FEM model simulated in Comsol® and calibrated to fit thermistors experimental data. The key aspect is to find an accurate and time-efficient strategy to reduce the possible impact of material parameter uncertainties on simulation results. Good agreement was reached with the proposed method on a packaged heater test-chip assembled with AuSn die-attach.

The thermal management of high-power semiconductor devices is generally critical and targets the lowest maximum junction temperature in operation to achieve longest component lifetime. A higher thermal conductivity of die attach material is always beneficial to reduce the chip temperature. New advances in die-attach materials for high power chips are nowadays based on silver-sintering technology.

The goal of this activity is to set-up a reliable procedure to extract the die-attach thermal conductivity from thermal simulations with accurate models calibrated with experimental data, including convection and radiation losses and the thermo-electric cooler.

The package configuration consists of a heater test-chip, suited for both heating and built-in temperature sensing, directly mounted with an AuSn die-attach layer on an AlN-substrate. The substrate is fixed to a Cu-W heat-spreader and controlled in temperature by the underlying thermo-electric-cooler (TEC). This is then mounted into a typical optoelectronics butterfly package. Finally, the package is connected to a water cooled aluminum plate by means of a thermal conductive paste (Figure 1).

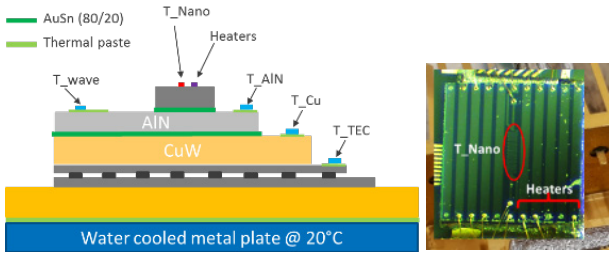

Figure 1: (left) Package configuration cross-section; (right) zoom on the heater test-chip assembled for die-attach evaluation purposes.

When simulating the thermal problem, a numerical accuracy of 3.2 K (~0.1% deviation on Temp. max. of 320 K) is achieved. Temperature deviations, on the contrary, between simulation and measurements are often well above 5 K.

To address these topics, we have identified two main strategies. At first, we calibrate the individual physics/component in the thermal model when possible with experimental data, if not at least with specification data verified by the component supplier.

The second step is to significantly reduce simulation time for each set of parameters from 75 min to around 7 min by adjusting solver settings, grid resolution and, while still retaining numerical accuracy.

Concerning the calibration of the package model, a basis for accurate modeling is to run parametric analysis (optimization) to estimate the die-attach thermal conductivity by matching experimental and simulated readings from the thermistors (Figure 1).

Comparison to experiments dataset #1 with full model are plotted in Figure 2. The resulting fitted curves are generated assuming a constant heat of 10.1 W on the Nanotest chip and by varying the thermo-electric cooler power from 0 W to 75 W. The temperature curve is accurate to within 2.17 K between simulated and measured test-chip on-board temperature sensor (T_Nano). This agreement has been achieved by calibrating the TEC and its thermal interface parameters.

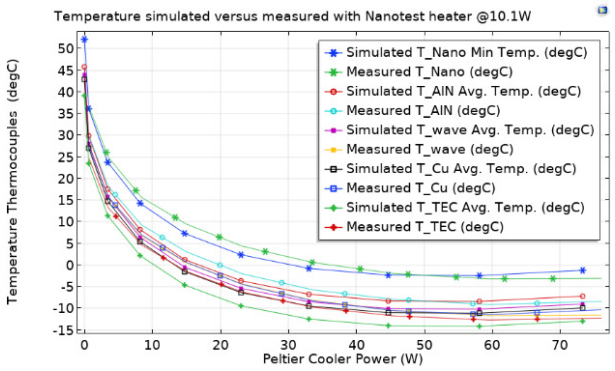

Figure 2: Thermistors temperature measured versus simulated with varying thermo-electric cooler power. Test-chip heater fixed at 10.1 W.

The non-linear multi-physics model fitted with dataset #1 was also used to predict correctly another experimental dataset #2, when keeping power constant at 60 W for the thermo-electric cooler and increasing the test-chip heating power from 0 W to 25 W. The results showed a good agreement, with a maximum deviation between simulated and measured on-board test-chip temperature of 1.14 K only. The defined procedure and modeling results so far achieved are therefore quite promising to enable calibration of thermal models.

As an outlook, we can use this approach to advance CSEM's contribution in the industry with relevance to areas involving silver sintering and other high thermal conductivity die-attach material properties verification. CSEM has conducted these investigations partially in the framework of the EU-consortium MIRPHAB [2] and partially in the recently started EU-project Heatpack [3].

[1] G. Spinola Durante, *et al.*, "Thermal Management Solutions for mid-IR Optoelectronics Packages", CSEM Scientific and Technical Report (2017) 36.

[2] MIRPHAB is an all-services integrated Pilot Line for the development of MID-IR photonics sensors in Europe. http://www.mirphab.eu/

[3] HEATPACK is an EU-Project Consortium developing "High thErmAl efficiency componenTs PACKages for space". http://www.heatpack.eu/